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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,544	07/01/2003	Thomas E. Pearson	42P13560D	3569

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EXAMINER	
GRAYBILL, DAVID E	
ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 03/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/612,544	PEARSON ET AL.	
	Examiner	Art Unit	
	David E. Graybill	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5-17 and 19-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-17 and 19-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

The reply filed on 11-17-4 is not fully responsive to the prior Office action because it fails to conform to the provisions of MPEP 714.03:

> 37 CFR 1.111. Reply by applicant or patent owner to a non-final Office action.
>
> (b) In order to be entitled to reconsideration or further examination, the applicant or patent owner must reply to the Office action. The reply by the applicant or patent owner must be reduced to a writing which distinctly and specifically points out the supposed errors in the examiner's action and must reply to every ground of objection and rejection in the prior Office action. The reply must present arguments pointing out the specific distinctions believed to render the claims, including any newly presented claims, patentable over any applied references. If the reply is with respect to an application, a request may be made that objections or requirements as to form not necessary to further consideration of the claims be held in abeyance until allowable subject matter is indicated. The applicant's or patent owner's reply must appear throughout to be a bona fide attempt to advance the application or the reexamination proceeding to final action. A general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references does not comply with the requirements of this section.
>
> (c) In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.
>
> Where a bona fide response to an examiner's action is filed before the expiration of a permissible period, but through an apparent oversight or inadvertence some point necessary to a complete response has been omitted - such as an amendment or argument as to one or two of several claims involved or signature to the amendment - the examiner, as soon as he or she notes the omission, should require the applicant to complete his or her response within a specified time limit (usually one month) if the period for response has already expired or insufficient time is left to take action before the expiration of the period. If this is done the application should not be held abandoned even though the prescribed period has expired.

Specifically, the 35 U.S.C. 112, second paragraph, rejection of claim 7 has not been addressed.

Because the response appears to be bona fide, but through an apparent oversight or inadvertence the response is incomplete, and in order to continue to afford applicant the benefit of compact prosecution, the requirement to complete the response within a one month time limit is waived, the amendment is entered, and the claims are examined on the merits.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

There is insufficient antecedent basis for the following:

Claim 7, "said grooves."

Claims 7 has not been rejected over the prior art because, in light of the 35 U.S.C. 112 rejection supra, there is a great deal of confusion and uncertainty as to the proper interpretation of the limitations of the claim; hence, it would not be proper to reject the claim on the basis of prior art. As stated in In re Steele, 305 F.2d 859, 134 USPQ 292 (CCPA 1962), a

rejection should not be based on considerable speculation about the meaning of terms employed in a claim or assumptions that must be made as to the scope of the claims. Also see In re Wilson, 424 F.2d 1382, 165 USPQ 494 (CCPA 1970) (if no reasonably definite meaning can be ascribed to certain claim language, the claim is indefinite, not obvious). See also MPEP 2143.03 and 2173.06.

In the rejections infra, generally, reference labels are recited only for the first recitation of identical claim elements.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 15, 16, 19, 20, 23, 24, 26, 29 and 32 are rejected under 35 U.S.C. 102(e) as being anticipated by Okada (6534726).

At column 9, line 5 to column 10, line 2; and column 11, line 1 to column 14, line 41, Okada discloses the following:

A method of manufacturing an interposer, the method comprising: creating a plurality of via holes 22/52,65 through a circuit board substrate 21 from a first surface of the substrate to a second surface of the substrate; creating a solid conductive column 57 through each of the via holes, the conductive column forming an electrical path from the first surface to the second surface; forming grooves 53 in the first surface and the second surface of the substrate between the via holes; coating the first surface and the second surface with a conductive material 55, 56; coupling the interposer between an electronic component package 12 and a circuit board 5; wherein the electronic component package includes a semiconductor die and the circuit board is a motherboard.

A method of manufacturing an interposer, the method comprising: creating a plurality of via holes through a circuit board substrate from a first surface of the substrate to a second surface of the substrate; creating a conductive path 54 through each of the via holes from the first surface to the second surface; and forming a plurality grooves in the first surface and

the second surface of the substrate between the via holes; wherein said forming a plurality of grooves comprises: forming a first plurality of grooves (any two grooves) in the first surface of the substrate; forming a second plurality of grooves (any two grooves other than the first plurality) in the first surface of the substrate, perpendicular to the first plurality of grooves; forming a third plurality of grooves in the second surface of the substrate (the first plurality of grooves); and forming a fourth plurality of grooves (the second plurality of grooves) in the second surface of the substrate, perpendicular to the third plurality of grooves; wherein said creating a conductive path through each of the via holes comprises forming a thin conductive layer on a surface of each of the via holes; wherein said creating a conductive path through each of the via holes comprises forming a solid conductive column 57 through each of the via holes; coupling the interposer between an electronic component package and a circuit board.

To further clarify the disclosure of forming grooves 53 in the first surface and the second surface of the substrate, the end portions of the grooves (illustrated but not labeled) are formed in the first and second surface of the substrate.

To further clarify the disclosure of forming grooves 53 between the via holes, the via holes are between the via holes and the grooves are in the via holes; hence the grooves are in and between the via holes.

To further clarify the disclosure of forming a second plurality of grooves perpendicular to the first plurality of grooves; and forming a fourth plurality of grooves perpendicular to the third plurality of grooves, it is noted that the grooves are three dimensional; therefore, each groove extends in a dimension perpendicular to every other groove.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point

out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 8, 12-14, 17 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okada (6534726).

Okada is applied as it is applied to claims 15, 16, 19, 20, 23, 24, 26, 29 and 32 supra.

Further, as cited supra, Okada discloses a method of manufacturing an interposer, the method comprising: creating a plurality of rows of via holes through a circuit board substrate from a first surface of the substrate to a second surface of the substrate, the first surface and the second surface being coated with a conductive material 55, 56; forming a conductive layer 54 in each of the via holes to provide a conduction path through each of the via holes from the conductive material on the first surface to the conductive material on the second surface; selectively removing "etching" some of the conductive material from the first surface to form a plurality of traces 55 on the first surface and the second surface, each trace in electrical contact with

the conductive layer in at least one of the via holes; and severing the substrate to produce a plurality of individual substrate members, by cutting the substrate through the middle of the via holes in each row of via holes and between each row of via holes along a particular axis "the line passing trough [sic] the centers of the solder accommodation holes"; forming grooves in the first surface and the second surface of the substrate between the via holes; wherein the conductive layer is a surface layer applied in each of the via holes; coupling at least one of the individual substrate members between an electronic component package and a circuit board; selectively removing some of the conductive material from the first surface to form a plurality of traces on the first surface and the second surface, each trace in electrical contact with the conductive column of one of the via holes; severing the substrate to produce a plurality of beams 11/51, by cutting the substrate through the middle of the via holes in each row of via holes and between each row of via holes along a particular axis "the line passing trough [sic] the centers of the solder accommodation holes."

To further clarify, Okada discloses beams 11/51 because Okada discloses principal horizontal supporting members 11/51.

However, Okada does not appear to explicitly disclose elongate beams.

Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose this particular shape because applicant has not disclosed that, in view of the applied prior art, the shape is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical, and it appears prima facie that the process would possess utility using another shape. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Also, Okada does not appear to explicitly disclose removing some of the conductive material from the second surface to form a plurality of traces on the second surface.

Nonetheless, as set forth supra, Okada discloses forming a plurality of traces 56 on the second surface, and further discloses removing "etching" some of the conductive material from the first surface to form a plurality of traces 55 on the first surface. Moreover, it would have been obvious to remove the conductive material from the second surface by "etching" to form the plurality of traces on the second surface.

Claims 1, 5, 6, 9-11, 21, 22, 25, 28, 30 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okada as applied to claims 8, 12-17, 19, 20, 23, 24, 26, 27, 29 and 32 supra, and further in combination with Lin (5222014).

As cited supra, Okada discloses a method comprising: creating a plurality of rows (illustrated in FIG.9 in the plane of the paper as the three parallel vertical rows defining the vertical sides of the four substrate members 11) of via holes 22/52,65 through a circuit board substrate 21 from a first surface 51A of the substrate to a second surface 51B of the substrate; forming a conductive layer 55, 56 on the first surface and on the second surface; forming a conductive path 54 through each of the via holes from the first surface to the second surface; and severing the substrate

through each row of via holes and between each row of via holes along a coordinate axis "the line passing trough [sic] the centers of the solder accommodation holes," to produce a plurality of substrate members 11/51; forming a plurality of elongate grooves in the first surface and in the second surface of the substrate, prior to said severing.

To further clarify the disclosure of severing the substrate between each row of via holes along a coordinate axis, Okada discloses this process at least at the horizontal row in the plane of the paper as illustrated in FIG. 9.

However, Okada does not appear to explicitly disclose elongate substrate members.

Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose this particular shape because applicant has not disclosed that, in view of the applied prior art, the shape is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical, and it appears prima facie that the process would possess utility using another shape. Indeed, it has been held that mere

dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Also, Okada does not appear to explicitly disclose affixing two or more of the elongate substrate members together in an edgewise orientation to form an interposer with a plurality of conductive vias arranged in a two-dimensional array; affixing two or more of the plurality of individual substrate members together to form an interposer as a substantially planar array; wherein each of the conductive columns has a composition of tin (Sn) and lead (Pb); wherein the composition comprises at least 81% lead (Pb); affixing two or more of the plurality of beams together in an array configuration to form the interposer.

Regardless, at column 3, lines 1-26; column 3, line 58 to column 2, line 49; column 5, lines 29-31; and column 6, lines 22-59, Lin discloses

affixing two or more of the substrate members 12, 20 together in an edgewise orientation to form an interposer with a plurality of conductive vias 24 arranged in a two-dimensional array (in the plane of the paper in FIG. 9); affixing two or more of the plurality of individual substrate members together to form an interposer as a substantially planar array; wherein each of the conductive "columns" 23 has a composition of tin (Sn) and lead (Pb); wherein the composition comprises at least 81% lead (Pb); affixing two or more of the plurality of beams 12/20 together in an array configuration to form the interposer. In addition, it would have been obvious to combine this disclosure of Lin with the disclosure of Okada because it would provide a densely packed device.

To further clarify the disclosure of Okada of affixing the substrate members in an edgewise orientation, it is noted that the disclosure of Okada is not limited to any particular absolute frame of reference, and there is at least one frame of reference wherein affixing the substrate members in a sideways orientation with one side forward is disclosed.

To further clarify the disclosure wherein the composition comprises at least 81% lead, Lin discloses, "This solder, for example, may be of an 80/20

Pb/Sn composition or any other workable solder alloy composition," and a composition comprising at least 81% lead is a workable solder alloy composition.

In any case, Lin discloses that lead concentration is a result-effective variable. Moreover, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed lead concentration limitation because applicant has not disclosed that, in view of the applied prior art, the limitation is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical, and it appears prima facie that the process would possess utility using another concentration. Indeed, it has been held that optimization of range limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See MPEP 2144.05(II): "Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. '[W]here the general conditions of a

claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.'" In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). See also In re Hoeschele, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969), Merck & Co. Inc. v. Biocraft Laboratories Inc., 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989), and In re Kulling, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990). As set forth in MPEP 2144.05(III), "Applicant can rebut a prima facie case of obviousness based on overlapping ranges by showing the criticality of the claimed range. 'The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range.' In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990). See MPEP § 716.02 - § 716.02(g) for a discussion of criticality and unexpected results."

Applicant's remarks filed 11-17-4 have been fully considered and are adequately addressed supra.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

For information on the status of this application applicant should check PAIR: Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alternatively, applicant may contact the File Information Unit at (703) 308-2733. Telephone status inquiries should not be directed to the examiner. See MPEP 1730VIC, MPEP 203.08 and MPEP 102.

Any other telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.
The fax phone number for group 2800 is (703) 872-9306.

David E. Graybill
Primary Examiner
Art Unit 2827

D.G.
2-Mar-05